What is claimed is:

1. A data sensing circuit for a magnetic memory cell, comprising:

a current source circuit that selectively supplies a current to the magnetic memory cell;

a first storage device selectively coupled to the magnetic memory cell that is configured to store a voltage representing a state of the magnetic memory cell;

a second storage device selectively coupled to the magnetic memory cell that is configured to store a voltage representing a state of the magnetic memory cell;

a differential voltage sense circuit coupled to the first and second storage devices that generates a sensed data output signal for the magnetic memory cell responsive to sensing a difference between voltages stored in the first and second storage devices; and

a control circuit that generates control signals to control the current source to supply current to the magnetic memory cell and to control the coupling of the first and second storage devices to the magnetic memory cell.

2. The data sensing circuit of Claim 1 wherein the current source circuit is configured to selectively apply a first current or a second current different from the first current responsive to a control signal from the control circuit.

3. The data sensing circuit of Claim 2 wherein the current source circuit comprises:

a plurality of transistors having serially connected current paths and gates connected to receive a first control signal;

a first transistor having a gate connected to receive a second control signal;

a second transistor coupled to the plurality of transistors and the first transistor;

a third transistor coupled to the magnetic memory cell having a gate coupled to a gate and a drain of the second transistor; and

wherein the first current or the second current are selected by selective activation of the first and second control signal.

4. The data sensing circuit of Claim 2 wherein the differential voltage sense circuit comprises a differential amplifier.

5. The data sensing circuit of Claim 2 further comprising a first switch transistor selectively coupling the first storage device to the magnetic memory cell and a second switch transistor selectively coupling the second storage device to the magnetic memory cell and wherein the control circuit is configured to generate control signals coupled to the switch transistors to control the coupling of the first and second storage devices to the magnetic memory cell.

6. The data sensing circuit of Claim 5 wherein the first storage device comprises a capacitor coupled to the first switch transistor and the second storage device comprise a capacitor coupled to the second switch transistor.

7. The data sensing circuit of Claim 2 wherein the magnetic memory cell comprises a magnetic tunnel junction.

8. The data sensing circuit of Claim 7 wherein the control circuit is configured to selectively couple the first storage device to the magnetic memory cell to store a voltage representing a data state of the magnetic memory cell to be sensed and to selectively couple the second storage device to the magnetic memory cell to store a voltage representing a known data state of the magnetic memory cell.

9. The data sensing circuit of Claim 8 wherein the control circuit is configured to select the first current when the first storage device is coupled to the magnetic memory cell and the second current when the second storage device is coupled to the magnetic memory cell.

10. The data sensing circuit of Claim 9 wherein the first current is lower than the second current and wherein the voltage stored in the first storage device is lower than the voltage stored in the second storage device when the data state of the magnetic memory cell corresponds to the known data state and wherein the voltage stored in the first storage device is greater than the voltage stored in the second storage device when the data state of the magnetic memory cell differs from the known data state.

11. A magnetic memory device including a plurality of magnetic memory cells and the data sensing circuit of Claim 10.

12. A magnetic memory device including a plurality of magnetic memory cells and the data sensing circuit of Claim 2.

13. A method of sensing data stored in a magnetic memory cell comprising:

supplying a first current to the magnetic memory cell to sense a first voltage corresponding to a resistance of the magnetic memory cell with the data stored in the magnetic memory cell;

storing determinate data in the magnetic memory cell;

supplying a second current to the magnetic memory cell to sense a second voltage corresponding to a resistance of the magnetic memory cell with the determinate data stored in the magnetic memory cell after storing the determinate data; and

sensing the data stored in the magnetic memory cell based on a difference between the first voltage and the second voltage.

14. The method of Claim 13 wherein sensing the data is followed by rewriting the sensed data in the magnetic memory cell.

15. The method of Claim 13 wherein the first current is less than the second current.

16. The method of Claim 13 wherein the first current is about 90 percent of the second current.

17. The method of Claim 16 wherein the determinate data is a "0" and wherein the first voltage is higher than the second voltage when the data stored in the magnetic memory cell is a "1".

18. The method of Claim 16 wherein the determinate data is a "0" and wherein the second voltage is higher than the first voltage when the data stored in the magnetic memory cell is a "0".

19. A data sensing circuit in a magnetic random access memory having a magnetic memory cell, the data sensing circuit comprising:

current source means for supplying a first current and/or a second current to the magnetic memory cell responsive to control signals;

first storage means for storing a first voltage corresponding to a resistance of the magnetic memory cell in response to a first switch signal;

second storage means for storing a second voltage corresponding to a resistance of the magnetic memory cell in response to a second switch signal; and

differential amplifier means for sensing data stored in the magnetic memory cell using a difference between the first voltage and the second voltage.

20. The data sensing circuit of Claim 19 wherein the current source means comprises:

a first transistor having a source connected to a power supply voltage, a drain and a gate, the drain and gate of the first transistor being connected to each other;

a second transistor having a source connected to the power supply voltage, a drain and a gate connected to the gate and drain of the first transistor;

a plurality of third transistors having current paths cascaded between the drain of the first transistor and a ground voltage and gates connected to receive a first control signal; and

a fourth transistor having a current path formed between the drain of the first transistor and the ground voltage and a gate connected to receive a second control signal, a current from the drain of the second transistor being supplied to the magnetic memory cell.

21. The data sensing circuit of Claim 19 wherein the first storage means comprises:

a switch transistor having a drain connected to the current source and the magnetic memory cell, a source and a gate connected to receive the first switch signal; and

a capacitor connected between the source of the switch transistor and a ground voltage.

22. The data sensing circuit of Claim 19 wherein the second storage means comprises:

a switch transistor having a drain connected to the current source and the magnetic memory cell, a source and a gate connected to receive the second switch signal; and

a capacitor connected between the source of the switch transistor and a ground voltage.

23. The data sensing circuit of Claim 19 wherein the first switch signal is activated when the first current from the current source is supplied to the magnetic memory cell.

24. The data sensing circuit of Claim 19 wherein the second switch signal is activated when the second current from the current source is supplied to the magnetic memory cell.

25. The data sensing circuit of Claim 19 wherein when the first voltage is higher than the second voltage, the differential amplifier means senses that data stored in the magnetic memory cell is '1'.

26. The data sensing circuit of Claim 19 wherein when the first voltage is lower than the second voltage, the differential amplifier means senses that data stored in the magnetic memory cell is '0'.

27. A magnetic random access memory comprising:

a memory cell array including magnetic memory cells arranged in rows and columns at intersections of word lines, bit lines and digit lines; and

sense amplifier means for sensing data in a selected magnetic memory cell,

wherein the sense amplifier means comprises:

current source means for supplying either one of a first current and a second current to the magnetic memory cell in response to control signals;

first storage means for storing a first voltage corresponding to a resistance of the magnetic memory cell in response to a first switch signal;

second storage means for storing a second voltage corresponding to a resistance of the magnetic memory cell in response to a second switch signal; and

differential amplifier means for sensing data stored in the magnetic memory cell using a difference between the first voltage and the second voltage.

28. The magnetic random access memory of Claim 27 wherein the first switch signal is activated when the first current from the current source is supplied to the selected magnetic memory cell.

29. The magnetic random access memory of Claim 28 wherein the first storage means comprises:

a switch transistor having a drain connected to the current source and the magnetic memory cell, a source and a gate connected to receive the first switch signal; and

a capacitor connected between the source of the switch transistor and a ground voltage.

30. The magnetic random access memory of Claim 27 wherein the second switch signal is activated when the second current from the current source is supplied to the magnetic memory cell.

31. The magnetic random access memory of Claim 30 wherein the second storage means comprises:

a switch transistor having a drain connected to the current source and the magnetic memory cell, a source and a gate connected to receive the second switch signal; and

a capacitor connected between the source of the switch transistor and a ground voltage.

32. A magnetic random access memory comprising:

a magnetic memory cell connected to a bit line;

a first transistor having a source connected to a power supply voltage, a drain connected to the bit line and a gate;

a second transistor having a source connected to the power supply voltage, a drain connected to the gate of the first transistor and a gate;

a first current path connected between the gates of the first and second transistors and a ground voltage and operated responsive to a first signal;

a second current path connected between the gates of the first and second transistors and the ground voltage and operated responsive to a second signal;

a first capacitor connected to the bit line;

a second capacitor connected to the bit line; and

a comparator that compares data values stored in the first and second capacitors.